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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,549	01/31/2001	Walter Vincent Dixon	RD-27,937	3210

6147 7590 01/12/2005

GENERAL ELECTRIC COMPANY
GLOBAL RESEARCH
PATENT DOCKET RM. BLDG. K1-4A59
NISKAYUNA, NY 12309

EXAMINER	
AZARIAN, SEYED H	
ART UNIT	**PAPER NUMBER**
2625	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/774,549	DIXON ET AL.	
	Examiner	Art Unit	
	Seyed Azarian	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,21,25,28,32-37,40,41,44 and 45* is/are rejected.

7)☒ Claim(s) *14-20,22-24,26,27,29-31,38,39,42 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

1. Applicant's arguments, filed 8/12/2004, see page 2 through page 4 of remarks, with respect to the rejection of claims 1-45 under 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Polichar et al (U.S. patent 6,205,199).

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-45, rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-43, of U.S. Patent No. 6,753,873. Each of the limitation set forth in the claims of the instant application is defined in the claims of the patent.

As an example consider claim 1, of current application, compared to claim 1, of patent application, it disclose at least one host processor executing operations with a host operating system, a host memory having a first section managed by the host operating system for storing the host operating system and executable program code (column 86, lines 5-6);

and a detector framing node communicating with said at least one host processor by way of said computer communication bus, said detector framing node receiving image data from an image detection system (flat panel), and controlling communication of the image data to the host memory over said computer communication bus (column 86, lines 17-22).

Claim 4, of current application, compared to claim 37, of patent application, it disclose the image system according to claim 27, wherein the host operating system is a non-real time operating system (column 89, lines 14-15).

Claim 9, of current application, compared to claim 32, of patent application, it disclose the image system according to claim 31, said detector framing node communicating with the at least one host processor over the PCI bus in parallel while said detector framing node receives the image data from the image detection system in serial (column 88, lines 61-65).

Claim 19, of current application, compared to claim 31, of patent application, it disclose the image system according to claim 27, wherein the computer communication bus is a PCI bus, and said detector framing node receives the image data independently from communication with the at least one host processor such that the detector framing node continues to receive the image data from the image detection system during interruption of the PCI bus (column 88, lines 54-60).

Claims 22-24, of current application, compared to claim 11, of patent application, it disclose the system according to claim 1, wherein said detector framing node selectably receives image data from a cardiac/surgical digital x-ray panel outputting at least 1024 columns.times x 1024 rows of data; a radiography digital x-ray panel outputting at least 2048 columns.times.2048 rows of data; or a mammography digital x-ray panel outputting at least 1920 columns.times.2304 rows of data (column 87, lines 5-10).

The other claims have similar correspondence to the patent application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-13, 21, 25, 28, 32-37, 40-41 and 44-45, are rejected under 35 U.S.C. 102(e) as being anticipated by Polichar et al (U.S. patent 6,205,199).

Regarding claim 1, Polichar discloses an image data acquisition system, comprising;

a host computer having at least one host processor executing operations with an operating system and a host memory storing data and a detector framing node being programmable to receive image data from a selected flat panel detector of a plurality of different flat panel detectors (column 12, lines 32-49, read out signal from the imager is synchronized with the

digitizer of the image processor via serial communications port and host memory, also column 4, lines 41-59, image processor received the digitized pixels transmitted by the serial interface drive of the controller);

And communicating the received image data to the host memory independent of the operating system (column 12, line 56 through column 13, line 10, image display within one frame time and available storage media used by the control unit, also Fig. 4, column 11, lines 3-18, communication port and host memory and finally column 23, lines 25-33).

Regarding claim 2, Polichar discloses the image data acquisition system according to claim 1, wherein the host computer runs a non-real time operating system, and said detector framing node continues to receive and store the image data from the selected flat panel detector during a lapse in communication with the host memory (see claim 1, and column 3, lines 33-51, displaying the full dynamic range of an image-capturing).

Regarding claim 3, Polichar discloses the data acquisition system according to claim 2, wherein the received image data is radioscopic image data and the selected panel detector includes an amorphous silicon photo-diode (Fig. 6, column 10, lines 37-59, flat panel includes amorphous silicon and column 15, lines 53-67, image is the radioscopic image).

Regarding claim 5, Polichar discloses the image data acquisition system according to claim 1, said detector framing node communicating the received image data with the host memory over a computer communication bus at a first clock frequency and receiving the image data from the selected flat panel detector over an image detection bus at a second clock frequency different from the first clock frequency (column 18, lines 13-31, separate clock timing signal).

Regarding claim 7, Polichar discloses the image data acquisition system according to claim 6, wherein the first clock frequency clocks parallel data of at least 33 MHz, and the second clock frequency clock serial data of at least 1GHz said detector framing (column 11, lines 20-31 also lines 49-67, 33 MHz).

Regarding claim 9, Polichar discloses the image data acquisition system according to claim 5, wherein the computer communication bus is a PCI bus (column 11, lines 3-18, communication port and host memory).

Regarding claim 10, Polichar discloses the image data acquisition system according to claim 9, wherein the image detection bus is an fiber data link and said detector framing node receives the image data from the selected flat panel detector over the optical fiber data link (column 7, lines 1-11, fiber optic).

Regarding claim 21, Polichar discloses the image data acquisition system according to claim 1, said detector framing node further comprising: a fiber optic interface converts the received serial image data into parallel image data (see claim 9, and column 20, lines 9-32).

Regarding claim 25, Polichar discloses the image data acquisition system according to claim 1, said detector framing node receiving the image data from a signal panel X-ray detection panel (column 9, lines 13-26).

Regarding claim 28, Polichar discloses the detector framing node comprising, a computer communication interface to communicate image data with a host memory of a host computer over a computer communication bus independently from control of a host processor of the host computer; and a control unit to receive a plurality of event instructions from the host computer through said computer communication interface, the event instructions selectively controlling

events in the detector framing node, a radiation generation system, or an image detection system (see claim 1, and column 4, lines 41-59, generating radiation, also column 14, line 65 through column 15, line 4).

Regarding claims 4, 6, 8, 11-12, 34-36 and 40-41, the arguments analogous to those presented for claims 1, 3, 5 and 7, are applicable.

Regarding claims 13, 33 and 37, the arguments analogous to those presented for claims 7 and 9 are applicable.

Regarding claims 32 and 44-45, the arguments analogous to those presented for claims 1, 10 and 21 are applicable.

Allowable Subject Matter

6. Claims 14-20, 22-24, 26-27, 29-31, 38-39 and 42-43 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claims.

Other prior art cited

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. patent (5,262,649) to Antonuk et al is cited for thin-film, flat panel, pixilated detector array for real-time digital imaging and dosimetry of ionizing radiation.

U.S. patent (4,672,454) to Cannella et al is cited for X-ray image scanner and method.

U.S. patent (4,996,413) to McDaniel et al is cited for apparatus and method for reading data from an image detector.

U.S. patent (6,205,199) to Polichar et al is cited for pixel-correlated digital X-ray imaging system.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seyed Azarian whose telephone number is (703) 306-5907. The examiner can normally be reached on Monday through Thursday from 6:00 a.m. to 7:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta, can be reached at (703) 308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR.
Status information about the PAIR system, see http:// pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Seyed Azarian

Patent Examiner

Group Art Unit 2625

January 9, 2005

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